UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/775,328	02/11/2004	Kiyoshi Kato	0756-7254	8545

31780 7590 01/24/2008

ERIC ROBINSON
PMB 955
21010 SOUTHBANK ST.
POTOMAC FALLS, VA 20165

EXAMINER	
FULK, STEVEN J	

ART UNIT	PAPER NUMBER
2891	

MAIL DATE	DELIVERY MODE
01/24/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

TH

Office Action Summary	Application No.	Applicant(s)	
	10/775,328	KATO ET AL.	
	Examiner	Art Unit	
	Steven J. Fulk	2891	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 January 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) *28-38* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *1/2/08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☒ Other: *Foreign Patent Document*.

DETAILED ACTION

Election/Restrictions

1. This application contains claims directed to the following patentably distinct species:

A. A semiconductor device comprising a light emitting element and a light receiving element (claims 1-27).

B. A semiconductor device comprising two light emitting devices (claims 28-38).

2. Newly submitted claims 28-38 are directed to a species that is patentably distinct from the invention originally claimed because claims 28-38 recite the mutually exclusive characteristics of such species. In addition, these species are not obvious variants of each other based on the current record.

There is an examination and search burden for these patentably distinct species due to their mutually exclusive characteristics. The species require a different field of search (e.g., searching different classes/subclasses or electronic resources, or employing different search queries); and/or the prior art applicable to one species would not likely be applicable to another species; and/or the species are likely to raise different non-prior art issues under 35 U.S.C. 101 and/or 35 U.S.C. 112, first paragraph.

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. **Accordingly, claims**

28-38 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03. Claims 1-27 are currently pending.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1 and 3 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 1 and 3 recite the limitation "the interlayer insulating film". There is insufficient antecedent basis for the limitation "the interlayer insulating film" in the claims.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1, 3, 5, 7, 9, 11, 16-21 and 23-27 are rejected under 35 U.S.C. 102(b) as being anticipated by Shimoda et al. (WO 00/57489, using US Patent 7,079,776 as the translation). The process limitations of forming the stack of the first and second semiconductor elements found in product

claims 5-8 invoke the product-by-process doctrine. Product-by-process claims are not limited to the manipulations of the recited steps, only the structure implied by the steps (*MPEP § 2113*). For example, anticipation of claims 5 and 6 does not require that the thin film transistor to be stacked by transferring a semiconductor element formed over a different substrate. Anticipation of claims 7 and 8 does not require the device to be formed by detaching a first semiconductor element formed over a first substrate and a second semiconductor element formed over a second substrate and by stacking the first semiconductor element and the second semiconductor element over an element substrate.

Shimoda discloses a semiconductor device comprising: a light emitting element (for example, fig. 1, E35 of '776) electrically connected to first semiconductor element including at least one thin film transistor (col. 4, lines 41-44), wherein the signal from the thin film transistor is inputted to the light emitting element; a light receiving element (D35) electrically connected to a second semiconductor element including at least one thin film transistor, wherein the signal from the light receiving element is inputted to the thin film transistor; a resin film (col. 3, lines 9-11, adhesive film between layers of 11-15 fig. 1; col. 6, line 67 - col. 7, line 5, adhesive disclosed to be resin) formed between the first semiconductor element and the second semiconductor element; wherein the first semiconductor element and the second semiconductor element are stacked with an interface (layer 14) and an interlayer insulating film interposed there between (fig. 1, window T

between E35 and D35; col. 5, lines 10-11, window T in layer 14 is made of glass and is formed between layers 15 and 13, thus an interlayer insulating film); wherein a first electric signal is converted to an optical signal in the light emitting element, wherein the optical signal is converted to a second electric signal in the light receiving element, and wherein a signal is transmitted and received between the first semiconductor element and the second semiconductor element by using the light emitting element and the light receiving element (col. 3, lines 12-30); wherein the light emitting element comprises a first electrode (fig. 5, 121), a second electrode (122), and an organic electro-luminescent layer laminated between the first electrode and the second electrode (col. 4, lines 44-49), and wherein the first electrode, the electro-luminescent layer, and the second electrode are overlapped each other (fig. 5); wherein the device is used in an electronic computer (col. 1, lines 7-12); wherein the first semiconductor element comprises a semiconductor layer (thin-film transistors are, by definition, inherently formed in a thin semiconductor film), and wherein the electro-luminescent layer is physically separated from the first semiconductor layer (fig. 2, light emitting element EXY is physically separated from thin-film circuitry 110); and further comprising a third semiconductor element comprising at least one thin film transistor (fig. 1, layer 12), wherein the first semiconductor element, the second semiconductor element and the third semiconductor element are stacked.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 2, 4, 6, 8, 10, 11, 16-21 and 23-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimoda et al. (WO 00/57489, using US Patent 7,079,776 as the translation) in view of Mueller '625.

Shimoda discloses all of the elements of the claim(s) as set forth in paragraph 6 above including an interlayer insulating film partially formed between and on either surface of the first and second semiconductor elements (window T), but the reference does not explicitly disclose the interlayer insulating film to be a metal oxide. Mueller teaches a stacked optoelectronic coupling element wherein a metal oxide is formed between the stacked elements (fig. 2, 3; col. 3, lines 15-17).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the metal oxide of Mueller as the insulating film in the optoelectronic device of Ovshinsky et al. One would have been motivated to do this because metal oxides were well known insulating materials used in optoelectronic devices due to their excellent insulation properties and their transparency (Mueller, col. 3, lines 15-17),

which would allow the device to perform its intended function by propagating the optical signal within the device.

9. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shimoda et al. (WO 00/57489, using US Patent 7,079,776 as the translation) in view of Ovshinsky et al. '471.

Shimoda discloses all of the elements of the claim(s) as set forth in paragraph 6 above, but the reference does not explicitly teach the semiconductor layer of the thin-film transistors to be a crystallized semiconductor layer. Ovshinsky teaches a semiconductor device (figs. 6A & 6B; col. 18, line 58 – col. 19, line 66) comprising stacked thin film semiconductor circuits each having a thin film transistor (fig. 6A, 232, 234; col. 2, line 39 – col. 3, line 21, DIFET thin film transistors), with an adhesive film (leveling film, 220) and an insulating film (236) formed between semiconductor circuits; wherein the first of the stacked semiconductor elements has a first crystallized layer (layer 158 of device 232; col. 2, lines 51-53, crystalline thin film devices) and wherein the second of the stacked semiconductor elements has a second crystallized semiconductor layer (layer 42 of device 234).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the crystallized semiconductor layers as the thin-film semiconductor layers of Shimoda. One would have been motivated to do this because it was well known in the art that crystallized

semiconductor layers improved the mobility of charge carriers in the thin-film transistors, thus improving the performance of the device.

Response to Arguments

10. Applicant's arguments with respect to claims 1-27 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven J. Fulk whose telephone number is (571) 272-8323. The examiner can normally be reached on Monday through Friday, 9:30am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bill Baumeister can be reached on (571) 272-1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

12. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SJF

Steven J. Fulk
Patent Examiner
Art Unit 2891

January 18, 2008

B. WILLIAM BAUMEISTER
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800